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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,290	06/07/2001	Yoshiyuki Yanagisawa	075834.00085	9540

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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	PAPER NUMBER
2894	

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04/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/876,290	YANAGISAWA ET AL.	
	Examiner	Art Unit	
	David E. Graybill	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,11-15 and 20* is/are pending in the application.

4a) Of the above claim(s) *3-6,12,13 and 15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,11,14 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1-22-09 has been entered.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 20 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There is insufficient antecedent basis for the following claim language:

Re claim 20: said mother substrate alignment structure.

In the rejections infra, generally, reference labels and other claim element identifiers are recited only for the first recitation of identical claim elements.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 11, 14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Woodman (5016138) and Bellaar (5861666).

At column 4, line 66 to column 5, line 21; column 5, line 54 to column 6, line 24; and at column 7, lines 18-27, Woodman discloses the following:

Re claim 1: A multilayer semiconductor device assembly jig for securing a plurality of semiconductor modules disposed within the assembly jig, comprising: at least one pair of opposed side walls 50 formed at a width slightly more than but substantially equal to a width of a rigid portion 22 of said plurality of semiconductor modules 46 located therebetween; the jig having a mother substrate alignment pins 26 located in the side walls for securing the mother substrate 80 to the jig; and further wherein each of the

plurality of semiconductor modules secured within the jig is comprised of one or more semiconductor chips 32 secured to a printed wiring board 22 that has electrical connections "coupling between layers" at a top and bottom surface thereof provided by "solder" located between adjacent printed wiring boards and wherein adjacent semiconductor modules are secured to one another "coupling between layers" by "solder" connections.

Re claim 11: A multilayer semiconductor device assembly jig for securing a plurality of semiconductor modules disposed within the assembly jig, comprising: at least two opposed side wails having a single stack of the semiconductor modules therebetween, the sidewalls being formed at a width slightly more than but substantially equal to a width of a rigid portion of said plurality of semiconductor modules; a mother substrate alignment structure comprised of pins located in the side walls; and further wherein each of the plurality of semiconductor modules secured within the jig is comprised of one or more semiconductor chips secured to a printed wiring board that has electrical connections at a top and bottom surface thereof provided by solder located between adjacent printed wiring boards and wherein adjacent semiconductor modules are secured to one another by solder connections between respective top and bottom surfaces thereof.

Re claim 14: An assembly jig for securing a plurality of semiconductor modules disposed within the assembly jig comprising: at least one pair of

substantially parallel opposed side wails secured to a solid base member 80, the sidewalls being formed at a width slightly more than but substantially equal to a width of a rigid portion of said plurality of semiconductor modules; the plurality of semiconductor modules secured within the jig each being comprised of one or more semiconductor chips each secured to a printed wiring board that has electrical contacts "coupling between layers" at a top and bottom surface thereof and solder located between adjacent printed wiring boards and wherein adjacent semiconductor modules are secured to one another by solder connections between respective top and bottom surfaces thereof.

Re claim 20: The multilayer semiconductor device assembly jig according to claim 1, wherein said mother substrate alignment structure is formed as a hole 54 that receives a pin member 26.

The following is further clarified:

Re claim 1: electrical connections "coupling between layers".

Re claim 11: electrical connections.

Re claim 14: electrical contacts "coupling between layers".

In particular, the solder coupling of Woodman is electrical connections and contacts because it is connections and contacts of, relating to, or utilizing devices constructed and working by the methods and principles of electronics.

However, Woodman does not appear to explicitly disclose the following:

Re claim 1: the electrical connections located between conductive pads on adjacent printed wiring boards.

Re claim 11: the electrical connections located between conductive pads on adjacent printed wiring boards.

Re claim 14: the electrical contacts located between conductive pads on adjacent printed wiring boards.

Nonetheless, at column 6, lines 25-49; and column 7, lines 9-63, Bellaar discloses the electrical connections 184 located between conductive pads 147, 140/154 on adjacent printed wiring boards "interposer".

To further clarify, Bellaar discloses pads 147, 140/154 because 147, 140/154 are portions of a conductive pattern on a solid-state electronic device for making external connection thereto; and portions of a conductive pattern on a chip or a printed circuit board designed for mounting or attaching a substrate or solid-state active electronic device, as "pad" is so defined in the U.S. Manual of Classification, Class 257, Glossary.

Furthermore, it would have been obvious to combine this disclosure of Bellaar with the disclosure of Woodman because it would facilitate provision of the solder connection and electrical connection of the circuit boards of Woodman.

Applicant's remarks filed 1-11-09 have been fully considered and are deemed moot in view of the new grounds of rejection.

For information on the status of this application applicant should check PAIR: Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

/David E Graybill/
Primary Examiner, Art Unit 2894